Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 20-29 are pending in the application, with claims 20 and 25 being the independent claims. Claims 1-19 were previously cancelled. Claims 20 and 25 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

Rejections of claims 20-29 as Anticipated by Walters

In the office action, the Examiner has maintained the rejection of claims 20-29 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,041,738 to Walters, Jr. ("Walters"). Based on the foregoing amendment and the following remarks, Applicants respectfully traverse.

Walters is directed to a CMOS clock generator that generates two CMOS phase clock signals having an adjustable overlap voltage. *See* Walters, col. 1, ll. 6-10. The clock generator 8 includes a first phase clock generating circuit 18 and a second phase clock generating circuit 22. *Id.*, col. 2, ll. 51-54, FIG. 1.

In Walters, the overlap voltage between the two CMOS phase clock signals is adjusted by selectively eliminating transistors in either or both of the first and second

phase clock generating circuits 18 and 22. Transistors are eliminated by blowing fuses using a laser cut. *Id.*, col. 3, ll. 18-21, 51-54. The selective elimination of transistors determines the rate at which an internal node within the first and second phase clock generating circuits 18 and 22 can charge or discharge, which in turn, affects the rate at which the CMOS phase clock signals transition between high and low output levels.

In particular, Walters teaches that to decrease the amount of overlap voltage, one or more transistors connected in parallel between an internal node of a phase clock generating circuit and ground may be eliminated, and, when all such transistors have been eliminated, one or more transistors connected in parallel between the internal node and the clock output of the other phase clock generating circuit may be eliminated until only one such transistor is remaining. *Id.*, col. 6, ll. 37-64. Alternatively, to increase the amount of overlap voltage, one or more transistors connected in parallel between the internal node of a phase clock generating circuit and the clock output of the other phase clock generating circuit may be eliminated. *Id.*, col. 6, l. 64-col. 7, l. 19.

Claim 20, as presently amended, is directed to a method for manufacturing a clock generator that generates two non-overlapping clock signals. The claimed method includes:

> providing an apparatus that includes a clock input portion, first and second clock outputs, a first feedback path for coupling said first clock output to said clock input portion, and a second feedback path for coupling said second clock output to said clock input portion;
>
> determining if first and second clock signals generated by said first and second clock outputs, respectively, have clock edges that are non-overlapping for a predetermined time T;
>
> adding one or more delay elements in series along said first and/or second feedback paths during manufacturing if said first and second clock signals

do not have clock edges that are non-overlapping for said predetermined time T.

Walters does not teach or suggest each of the foregoing features of claim 20. Most significantly, perhaps, Walters does not teach or suggest "a method for manufacturing a clock generator that generates two *non-overlapping* clock signals" at all. Rather, Walters is directed to clock generator in which an amount of voltage overlap between two CMOS phase clock signals may be adjustably increased or decreased, but not eliminated. This is graphically illustrated, for example, in FIGS. 3(a) , 3(b), and 3(c) of Walters. Walters nowhere teaches or suggests the generation of non-overlapping clock signals, and for this reason alone cannot be an anticipatory reference.

Additionally, Walters does not teach or suggest "adding one or more delay elements in series along said first and/or second feedback paths" as recited in claim 8. As noted above, in Walters, the fuse/transistor combinations are connected *in parallel* between an internal node of each of the two phase clock generating circuits and ground and between an internal node of each of the two phase clock generating circuits and the clock output of the other phase clock generating circuit. In accordance with this structure, blowing a fuse corresponding to a transistor changes the "channel width" of the single transistor equivalent of the combination of transistors. *See* Walters, col. 6, ll. 12-17. This is simply not the same thing as "adding one or more delay elements in series along said first and/or second feedback paths" as recited in claim 8, for at least the reasons that (1) removing a transistor in Walters does not necessarily add any sort of delay along lines 24 or 26 in Walters (the Examiner has equated these lines to the recited feedback paths), and (2) the fuse/transistor combinations which the Examiner has equated to "delay elements" are arranged in parallel, not in series.

Since Walters does not teach or suggest each and every limitation of claim 20, it cannot anticipate that claim. Accordingly, the Examiner's rejection of claim 20 under 35 U.S.C. § 102(b) is traversed and Applicants respectfully request that the rejection be withdrawn. Furthermore, dependent claims 21-24 are also not anticipated by Walters for at least the same reasons as independent claim 20 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 21-24 under 35 U.S.C. § 102(b) is also traversed and Applicants respectfully request that the rejection be withdrawn.

Claim 25, as presently amended, is directed to a method for manufacturing a clock generator that generates two non-overlapping clock signals. The claimed method includes:

> providing an apparatus that includes a clock input portion, first and second clock outputs, a first feedback path for coupling said first clock output to said clock input portion, and a second feedback path for coupling said second clock output to said clock input portion;
>
> determining if first and second clock signals generated by said first and second clock outputs, respectively, have clock edges that are non-overlapping for a predetermined time T; and
>
> removing one or more delay elements in series along said first and/or second feedback paths during manufacturing if said first and second clock signals do not have clock edges that are non-overlapping for said predetermined time T.

Walters does not teach or suggest each of the foregoing features of claim 25. For example, as discussed above in reference to claim 20, because Walters describes a clock generator in which an amount of voltage overlap between two CMOS phase clock signals may be adjustably increased or decreased, but not eliminated, Walters does not teach or suggest "a method for manufacturing a clock generator that generates two *non-*

overlapping clock signals" at all. Furthermore, Walters does not teach or suggest "removing one or more delay elements in series along said first and/or second feedback paths" as recited in claim 8 for at least the reasons that (1) removing a transistor in Walters does not necessarily reduce any sort of delay along lines 24 or 26 in Walters (the Examiner has equated these lines to the recited feedback paths), and (2) the fuse/transistor combinations which the Examiner has equated to "delay elements" are arranged in parallel, not in series.

Since Walters does not teach or suggest each and every limitation of claim 25, it cannot anticipate that claim. Accordingly, the Examiner's rejection of claim 25 under 35 U.S.C. § 102(b) is traversed and Applicants respectfully request that the rejection be withdrawn. Furthermore, dependent claims 26-29 are also not anticipated by Walters for at least the same reasons as independent claim 25 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 26-29 under 35 U.S.C. § 102(b) is also traversed and Applicants respectfully request that the rejection be withdrawn.

Rejections of claims 20, 21, 25 and 26 as Anticipated by Tazaki

In the office action, the Examiner has also maintained his rejection of claims 20, 21, 25 and 26 under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent JP 2-124627 to Tazaki ("Tazaki"). Based on the foregoing amendment and the following remarks, Applicants respectfully traverse.

Tazaki is directed to a clock driver circuit for obtaining complementary clock signals having a variable delay time. In particular, Tazaki teaches a clock driver circuit that includes two delay time selection circuits 5 and 8 having control terminals 6 and 9,

respectively. *See* Tazaki, FIG. 1. Each delay time selection circuit 5 and 8 includes a decoder circuit 18, switches 16 and 17, and delay circuits 13, 14 and 15. *See* Tazaki, FIG. 3. Control signals 9 are applied to decoder circuit 18 during operation of the device to controls switches 16 and 17 within the delay time selection circuit to either connect to or short-circuit delay circuits 13 and 14, respectively.

In contrast to the programming-based technique taught by Tazaki, which is implemented during operation of the device, the present invention uses a manufacturing-based technique to ensure generation of two non-overlapping clock signals. In particular as recited in claims 20 and 25, the present invention is directed to a "*method for manufacturing* a clock generator that generates two non-overlapping clock signals." The method includes "adding one or more delay elements in series along said first and/or second feedback paths *during manufacturing* " (claim 20) or "removing one or more delay elements in series along said first and/or second feedback paths *during manufacturing*" (claim 25). This feature is neither taught nor even suggested by Tazaki, which as illustrated above is directed to a *programming-based* technique for determining delay time between two clocks.

Since Tazaki does not teach or suggest each and every limitation of claim 20 or claim 25, it cannot anticipate those claims. Accordingly, the Examiner's rejection of claims 20 and 25 under 35 U.S.C. § 102(b) is traversed and Applicants respectfully request that the rejection be withdrawn. Furthermore, dependent claims 21 and 26 are also not anticipated by Tazaki for at least the same reasons as the independent claims from which they depend and further in view of their own respective features.

Accordingly, the Examiner's rejection of claims 21 and 26 under 35 U.S.C. § 102(b) is also traversed and Applicants respectfully request that the rejection be withdrawn.

Rejections under 35 U.S.C. § 103

In the office action, the Examiner maintained his rejection of claims 22-24 and 27-29 under 35 U.S.C. § 103(a) as obvious over Tazaki in view of Walters. Based on the foregoing amendment and the following remarks, Applicants respectfully traverse.

Independent claim 20 recites in part the feature of "adding one or more delay elements in series along said first and/or second feedback paths during manufacturing" and independent claim 25 recites in part the feature of "removing one or more delay elements in series along said first and/or second feedback paths during manufacturing". These features are neither taught by Tazaki, which as illustrated above is directed to a programming-based technique for determining delay time between two clocks, nor by Walters, which as illustrated above, does not teach or suggest adding/removing delay elements in series along feedback paths.

Furthermore, contrary to the Examiner's assertion, one of ordinary skill in the art would not have been motivated to replace the series of switches in each of the delay time selection circuits 5 and 8 of Tazaki's clock driver circuit with Walter's fuse/transistor pairs, since blowing a fuse in Tazaki's clock driver circuit would create a permanent open circuit, thereby rendering Tazaki's circuit inoperable. Moreover, because Tazaki relies on programmable switches which are controlled during operation of a finished device, it

teaches away from the use of any manufacturing-based solution for generating two non-overlapping clock signals.

Consequently, the combination of Tazaki and Walters fails to render obvious independent claims 20 or 25. Dependent claims 22-24 and 27-29 are also not rendered obvious by this combination for at least the same reasons as the independent claims from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 22-24 and 27-29 under 35 U.S.C. § 103(a) is traversed and Applicants respectfully request that the rejection be withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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